## REMARKS/ARGUMENTS

Claims 1, 6, 26, 29-30, 32, 34-35, 38-39 are pending in the present application. Claims 2-5, 7-25, 27-28, 31, 33, 36-37, 40-53 are canceled; no claims were amended; and no claims were added. The listing of the claims beginning on page 2 of this response replaces all prior versions, and listings, of claims in the application.

## I. Double Patenting

The Examiner states the following:

> Claims 1, 32 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 6,21,25 of copending Application No. 10/675,777 (hereinafter '777), now patented as USPN: 7,395,527.
>
> Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following observations.
>
> **As per instant claims** 1, 32, '777 claims 6,21,25 also recite determining for a instruction during execution for a association of an indicator associated with receiving a bundle or instruction in a instruction cache; associating a counter based on such determination and incrementing a counter in response to the indicator association with the instruction or event associated with the indicator. The event counting and instruction cache as recited by '777 are construed as obvious representation to a runtime indicator (leading to a counter increment, in which incrementing is count of number of instructions execution) and sending from the cached instruction for execution of the instant claims. Further, '777 does not recite 'spare bit' for indicator identifying whether the instruction is to be monitored, but based on the indicator received into a cache, a bit type implementation as a slot within an received instruction would have been a obvious feature, enabling a monitoring to receive the instruction and increment a counter based on '777 paradigm.
>
> Claims 1, 32 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 3, 17 of copending Application No. 10/675872 (hereinafter '872), now patented as USPN: 7,373,637.
>
> **As per instant claims** 1, 32, '872 claims 3, 17 also recite instruction to be monitored and sent from cache instruction, determining whether an instruction in execution is related with an runtime range 'indicator'; and counting each event associated with the instruction if the instruction is associated with that range indicator. Even though '872 does not recite receiving bundle into a instruction cache and sending the received bundle for execution, said limitation of instruction with associated indicator would made the instruction cache receiving and

sending obvious steps within runtime based on instruction being cached in view of the above known concept, and the incrementing responsive to association of instruction with the indicator. Even though '872 explicitly recites that the indicator is a location within contiguous range, this location-within- range limitation would be a obvious representation of any runtime indicator that would characterizes as an event deemed for the counter to be incremented (in which incrementing in terms of count of number of instructions execution) in view of the above association determination. Further, '872 does not recite 'spare bit' for indicator identifying whether the instruction is to be monitored, but based on the indicator received into a cache, a bit type implementation as a slot within an received instruction would have been a obvious feature, enabling a monitoring to receive the instruction and increment a counter based on '872 paradigm.

Claims 1, 32 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 12,2 3 of copending Application No. 10/682,385 (hereinafter '385).

**As per instant claims 1, 32,** '385 claims 1, 12, 23 also recite executing instructions and detecting indicators that specify counting of events associated with the executing (Note: even though '385 recites data values in memory specifying counting event, a runtime event such as those memory indicators can be analogous to on runtime indicator of the instant claim); and counting each event associated with indicators. At the time the invention was made, expediting execution using instruction cache associated with profiling was known concept. Even though '385 does not recite receiving bundle into a instruction cache and sending the received bundle for execution, said limitation of executing instructions associated with indicators would made the instruction cache reception and the sending obvious steps within runtime based on instruction being cached in view of the above known concept, and the incrementing responsive to association of instruction with the indicator. Even though '385 explicitly recites that counting events associated with execution based on detection of value indicators, this limitation would be a obvious representation of any runtime indicator that would characterizes as an event deemed for the counter to be incremented (in which incrementing is in terms of count of number of executions) in view of the above association determination. Further, '385 does not recite 'spare bit' for indicator identifying whether the instruction is to be monitored, but based on the indicator received into a cache, a bit type implementation as a slot within an received instruction would have been a obvious feature, enabling a monitoring to receive the instruction and increment a counter based on '385 paradigm

Claims 6,26,29-30, 34-35, 38-39 are also rejected for not curing to the conflicting issues as raised above.

Final Office Action dated June 15, 2010, pages 3-5.

In response, Applicants are filing three Terminal Disclaimers herewith. In light of the Terminal Disclaimers, withdrawal of the rejection is respectfully requested.

## II. Allowable Subject Matter

> Claims 1, 32 stand rejected in the Double patenting Rejection as set forth above; yet contain allowable subject matter in view of the teachings provided via Fig. 31 of the Specifications; but would be allowable if rewritten in a form including or reasonably conveying functionality of all of the constituents (see Note below) of the 'instruction cache unit' described in the pertinent section. The allowable subject matter revolves around the following scenario, pending the inclusion of *range registers, counter increment based on range execution* of Figure 31:
>
> A instruction cache unit (ICU) having a counter therein that is incremented responsive to this ICU receiving of a spare bit and an instruction, the spare bit as an indicator to be determined by the ICU as to whether the instruction to be one to be monitored by a performance monitor unit, wherein upon receiving a signal from the ICU in response to the determination, the performance unit increments a counter implemented inside the ICU in conjunction with sending by the ICU of the instruction to a functional unit.
>
> Note: the constituents of the ICU depicted in **Figure 31,** deemed allowable based on the previously considered Appeal Brief (per 913012009), based on the emphasis expressed therein by the arguments regarding the Inventor's particular way of implementing an "instruction cache unit" being distinguishable over any conventional instruction cache, include (see Specifications):
>
> *In this example, program 3100 includes instruction range 3102 and 3104. Each of these ranges has been identified as ones of interest for monitoring. Each of these ranges is set within an instruction unit, such as instruction cache unit 214 in FIG. 2. Each range is used to tell the processor the number of instructions executed in a range, as well as the number of times a range is entered during execution of program 3100.*
>
> *Instruction cache unit 3106 uses range registers 3108 to define instruction ranges. These registers may be existing registers or instruction cache unit 3106 may be modified to include registers to define instruction ranges. These ranges may be based on addresses of instructions. Additionally, range registers 3108 may be updated by various debugger programs and performance tools.*
>
> *If an instruction is executed in a range, such as instruction range 3102 or instruction range 3104, a counter is incremented in instruction cache unit 3106.*

Final Office Action dated June 15, 2010, pages 5-6.

Applicants respectfully submit that the Examiner's requirement that the Applicants rewrite the claims is improper. The Examiner has not cited any Rule, Law or Prior Art that

would necessitate amendments to the claims. Instead, the Examiner's attempt to require additional limitations amounts to an improper limitation on the scope of the claims.

Because the Examiner has not cited any Rule, Law or Prior Art that would necessitate amendments to the claims, the Applicants respectfully decline to amend the claims.

## III. Conclusion

It is respectfully urged that the subject application is in condition for allowance.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: September 14, 2010

Respectfully submitted,

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